What is claimed is:

1. A double gate MOS transistor comprising:

a substrate active region defined in a semiconductor substrate;

a transistor active region located over the substrate active region and overlapped with the substrate active region;

at least one semiconductor pillar penetrating the transistor active region and being in contact with the substrate active region, the at least one semiconductor pillar supporting the transistor active region so that the transistor active region is spaced apart from the substrate active region;

at least one bottom gate electrode substantially filling a space between the transistor active region and the substrate active region, the at least one bottom gate electrode being insulated from the substrate active region, the transistor active region and the semiconductor pillar; and

at least one top gate electrode crossing over the transistor active region, and having at least one end that is in contact with a sidewall of the at least one bottom gate electrode, the at least one top gate electrode overlapping with the bottom gate electrode and being insulated from the transistor active region.

2. The double gate MOS transistor according to claim 1, wherein the at least one semiconductor pillar is a single semiconductor pillar penetrating a portion of the transistor active region and the at least one bottom gate electrode is a single bottom gate electrode.

3. The double gate MOS transistor according to claim 1, wherein the at least one semiconductor pillar is a single semiconductor pillar dividing the transistor active region into a first transistor active region and a second transistor active region, and dividing the bottom gate electrode into a first bottom gate electrode and a second bottom gate electrode.

4. The double gate MOS transistor according to claim 3, wherein the at least one top gate electrode includes a first top gate electrode crossing over the first transistor active region and a second top gate electrode crossing over the second transistor active region, the first and second top gate electrodes overlapping with the

first and second bottom gate electrodes respectively, at least one end of the first top gate electrode contacting a sidewall of the first bottom gate electrode, and at least one end of the second top gate electrode contacting a sidewall of the second bottom gate electrode.

5. The double gate MOS transistor according to claim 1, wherein the at least one semiconductor pillar includes a central semiconductor pillar intersecting the central portions of the transistor active region and the bottom gate electrode and a first semiconductor pillar and a second semiconductor pillar located at opposite sides of the central semiconductor pillar respectively, the transistor active region between the first and second semiconductor pillars being divided into a first transistor active region and a second transistor active region separated by the central semiconductor pillar, and the bottom gate electrode between the first and second semiconductor pillars being divided into a first bottom gate electrode and a second bottom gate electrode separated by the central semiconductor pillar.

6. The double gate MOS transistor according to claim 5, wherein the at least one top gate electrode includes a first top gate electrode crossing over the first transistor active region and a second top gate electrode crossing over the second transistor active region, the first and second top gate electrodes overlapping with the first and second bottom gate electrodes respectively, at least one end of the first top gate electrode being in contact with a sidewall of the first bottom gate electrode, and at least one end of the second top gate electrode being in contact with a sidewall of the second bottom gate electrode.

7. The double gate MOS transistor according to claim 1, wherein the at least one semiconductor pillar includes a first semiconductor pillar and a second semiconductor pillar located on both edges of the transistor active region and the bottom gate electrode respectively.

8. The double gate MOS transistor according to claim 7, wherein the at least one top gate electrode includes first and second parallel top gate electrodes crossing over the transistor active region, at least one end of the first and second top gate electrodes being in contact with sidewalls of the bottom gate electrode.

9. A double gate MOS transistor comprising:

an isolation layer formed at a predetermined region of a semiconductor substrate to define a substrate active region;

a transistor active region disposed over the substrate active region and overlapped with the substrate active region;

a central semiconductor pillar intersecting the central portion of the transistor active region to divide the transistor active region into a first transistor active region and a second transistor active region and to contact the substrate active region, the central semiconductor pillar supporting the first and second transistor active regions so that the first and second transistor active regions are spaced apart from the substrate active region;

a first bottom gate electrode substantially filling a space between the first transistor active region and the substrate active region, the first bottom gate electrode being insulated from the substrate active region, the first transistor active region and the semiconductor pillar;

a second bottom gate electrode substantially filling a space between the second transistor active region and the substrate active region, the second bottom gate electrode being insulated from the substrate active region, the second transistor active region and the semiconductor pillar;

a first top gate electrode crossing over the first transistor active region and having both ends that are in contact with sidewalls of the first bottom gate electrode; and

a second top gate electrode crossing over the second transistor active region and having both ends that are in contact with sidewalls of the second bottom gate electrode, the first and second top gate electrodes overlapping with the first and second bottom gate electrodes respectively.

10. The double gate MOS transistor according to claim 9 further comprising an isolation impurity region formed at a surface of the substrate active region contacting the central semiconductor pillar, the isolation impurity region having a different conductive type from the semiconductor substrate.

11. The double gate MOS transistor according to claim 9, wherein a top

surface of the isolation layer is located at a same level as a top surface of the substrate active region or lower than the top surface of the substrate active region.

12. The double gate MOS transistor according to claim 9, further comprising:

a common drain region formed at the central semiconductor pillar as well as the first and second transistor active regions between the first and second top gate electrodes;

a first source region formed at the first transistor active region that is adjacent to the first top gate electrode and opposite the common drain region; and

a second source region formed at the second transistor active region that is adjacent to the second top gate electrode and opposite the common drain region.

13. A double gate MOS transistor comprising:

an isolation layer formed at a portion of a semiconductor substrate to define a substrate active region;

a transistor active region disposed over the substrate active region and overlapped with the substrate active region;

a first semiconductor pillar and a second semiconductor pillar placed at both sides of the transistor active region respectively, the first and second semiconductor pillars contacting the substrate active region;

a central semiconductor pillar intersecting a central portion of the transistor active region to divide the transistor active region into a first transistor active region and a second transistor active region and to contact the active region, the central semiconductor pillar supporting the first and second transistor active regions so that the first and second transistor active regions are spaced apart from the substrate active region;

a first bottom gate electrode substantially filling a space between the first transistor active region and the substrate active region, the first bottom gate electrode being insulated from the substrate active region, the first transistor active region, the first semiconductor pillar and the central semiconductor pillar;

a second bottom gate electrode substantially filling a space between the second transistor active region and the substrate active region, the second bottom gate electrode being insulated from the active region, the second transistor active region, the second semiconductor pillar and the central semiconductor pillar;

a first top gate electrode crossing over the first transistor active region and having both ends that are in contact with sidewalls of the first bottom gate electrode; and

a second top gate electrode crossing over the second transistor active region and having both ends that are in contact with sidewalls of the second bottom gate electrode, the first and second top gate electrodes overlapping with the first and second bottom gate electrodes respectively.

14. The double gate MOS transistor according to claim 13 further comprising isolation impurity regions formed at the substrate active region contacting the first and second semiconductor pillars and the central semiconductor pillar, the isolation impurity regions having a different conductive type from the semiconductor substrate.

15. The double gate MOS transistor according to claim 13, wherein a top surface of the isolation layer is located at a same level as that of the substrate active region or is lower than a level of the substrate active region.

16. The double gate MOS transistor according to claim 13, further comprising:

a common drain region formed at the central semiconductor pillar as well as the first and second transistor active regions between the first and second top gate electrodes;

a first source region formed at the first semiconductor pillar and the first transistor active region that is adjacent to the first top gate electrode and opposite the common drain region; and

a second source region formed at the second semiconductor pillar and the second transistor active region that is adjacent to the second top gate electrode and opposite the common drain region.

17. A double gate MOS transistor comprising:

an isolation layer formed at a portion of a semiconductor substrate to define a substrate active region;

a transistor active region disposed over the substrate active region and overlapped with the substrate active region;

a first semiconductor pillar and a second semiconductor pillar disposed at both sides of the transistor active region respectively, the first and second semiconductor pillars contacting the substrate active region;

a bottom gate electrode substantially filling a space between the transistor active region and the substrate active region, the bottom gate electrode being insulated from the substrate active region, the transistor active region, the first semiconductor pillar and the second semiconductor pillar; and

first and second parallel top gate electrodes crossing over the transistor active region, each of the first and second top gate electrodes having both ends that are in contact with sidewalls of the bottom gate electrode, and the first and second top gate electrodes being located between the first and second semiconductor pillars to overlap with the bottom gate electrode.

18. The double gate MOS transistor according to claim 17 further comprising isolation impurity regions formed at the substrate active region contacting the first and second semiconductor pillars, the isolation impurity regions having a different conductive type from the semiconductor substrate.

19. The double gate MOS transistor according to claim 17, wherein a top surface of the isolation layer is located at a same level as that of the substrate active region or is lower than a level of the substrate active region.

20. The double gate MOS transistor according to claim 17, further comprising:

a common drain region formed at the transistor active region between the first and second top gate electrodes;

a first source region formed at the first semiconductor pillar and the transistor active region that is adjacent to the first top gate electrode and opposite the common drain region; and

a second source region formed at the second semiconductor pillar and the transistor active region that is adjacent to the second top gate electrode and opposite the common drain region.

21. A method of manufacturing a double gate MOS transistor, the method

comprising:

sequentially forming a first sacrificial layer, a semiconductor layer and a bottom hard mask layer on a semiconductor substrate;

forming at least one semiconductor pillar penetrating the bottom hard mask layer, the semiconductor layer and the first sacrificial layer to contact a portion of the semiconductor substrate;

forming a top hard mask layer on the semiconductor substrate having the semiconductor pillar;

successively patterning the top hard mask layer and the bottom hard mask layer to form a hard mask pattern that covers the semiconductor pillar;

successively etching the semiconductor layer, the first sacrificial layer and the semiconductor substrate using the hard mask pattern as an etching mask, thereby forming a first sacrificial layer pattern and a transistor active region that are sequentially stacked and in contact with the semiconductor pillar and simultaneously forming a trench region that defines an active region under the hard mask pattern;

selectively removing the first sacrificial layer pattern to form an undercut region under the transistor active region;

forming a second sacrificial layer pattern substantially filling the undercut region;

forming a recessed isolation layer in the trench region to expose a sidewall of the second sacrificial layer pattern;

selectively removing the second sacrificial layer pattern and the hard mask pattern to form another undercut region under the transistor active region;

forming a gate insulating layer on a surface of the transistor active region, a top surface of the active region and a surface of the semiconductor pillar;

forming a conductive layer substantially filling the other undercut region on the semiconductor substrate having the gate insulating layer; and

patterning the conductive layer to form at least one top gate electrode crossing over the transistor active region and overlapping with the other undercut region and to form a bottom gate electrode remaining in the other undercut region and contacting at least one end of the top gate electrode.

22. The method according to claim 21, wherein the first sacrificial layer is formed of a single crystalline semiconductor layer having an etching selectivity with

respect to the semiconductor substrate and the semiconductor layer.

23. The method according to claim 22, wherein the single crystalline semiconductor layer is formed of a silicon germanium (SiGe) layer.

24. The method according to claim 21, wherein the semiconductor layer is formed of a single crystalline silicon layer.

25. The method according to claim 21, wherein the bottom hard mask layer is formed of a silicon nitride layer.

26. The method according to claim 21, wherein forming the at least one semiconductor pillar comprises:

successively patterning the bottom hard mask layer, the semiconductor layer and the first sacrificial layer to form a hole that exposes a portion of the semiconductor substrate; and

filling the hole with a semiconductor material using a selective epitaxial growth technique.

27. The method according to claim 26 further comprises implanting impurity ions having a different conductivity type from the semiconductor substrate into the exposed semiconductor substrate before filling the hole with the semiconductor material, thereby forming an isolation impurity region.

28. The method according to claim 26, wherein filling the hole with the semiconductor material comprises:

growing a preliminary semiconductor pillar on the inner walls of the hole using a selective epitaxial growth technique, the preliminary semiconductor pillar being grown to not completely fill the hole;

annealing the preliminary semiconductor pillar; and then

filling the hole with the semiconductor material using the selective epitaxial growth technique.

29. The method according to claim 28, wherein the annealing is performed

using argon gas at a temperature of about 900 °C.

30. The method according to claim 28, wherein the annealing is performed using hydrogen gas at a temperature of from about 600 °C to 1000 °C.

31. The method according to claim 28, wherein the annealing is performed using a laser.

32. The method according to claim 21, wherein the semiconductor pillar is formed of the same material layer as the semiconductor layer.

33. The method according to claim 21, wherein the top hard mask layer is formed of the same material layer as the bottom hard mask layer.

34. The method according to claim 21, wherein forming the second sacrificial layer pattern comprises:

forming a second sacrificial layer filling the undercut region on surface of the semiconductor substrate where the first sacrificial layer pattern was removed; and

etching the second sacrificial layer to expose inner walls of the trench region to leave the second sacrificial layer only in the undercut region.

35. The method according to claim 34, wherein the second sacrificial layer is formed of the same material layer as the hard mask pattern.

36. The method according to claim 21 further comprising implanting impurity ions into the transistor active region using the top gate electrode as an ion implantation mask to form source/drain regions.